The Design and Simulations of Carrier Recovery Circuits with Pre-assured 2nd order Digital Loop Filter

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***Abstract* —Carrier recovery circuit is always a crucial issue in circuit designs, especially in mobile communications and many other applications which will produce phase shift or frequency drift due to relative activity or environments variations. For keeping track of these crucial changing parameters, a synchronization circuit with 2nd order digital loop is generally applied for its simplicity, flexibility, and fast settling time. In this paper, a typical second order digital loop filter with pre-assured stable convergence triangle from Jury criteria is developed, which can then be directly applied in many circuit designs with phase or frequency drifts by simply adjusting two digital loop parameters. The convergence property and the effectiveness of this digital loop filter and its applied circuits with derived recursive formulations are well studied and simulated. This simple and direct scheme can easily tell the designers the stable convergence contours under specific circumstances in the whole design stages.**

I. INTRODUCTION

The importance of synchronization circuits in modern circuit designs is indisputable and is always a crucial issue in circuit designs, especially in mobile communications and many applications which will produce phase shift or frequency drift due to relative activity, components aging, or environments variations. Therefore, a fast, stable, and flexible tracking loop design is always a necessity. For example, the Doppler effects will be generated while the systems are in relatively mobile conditions. And it will be much more severe, especially when the systems are operating in higher frequency bands, e.g., a few kHz drift will be normal for Ku-band satellite communications. In addition, the inherent frequency variations of crystal oscillator no less than 10 ppm in the whole operating frequency band and temperature range due to components aging and environments are generally happened, which will cause relatively large phase shift or frequency drift if a specific synchronization circuit is not applied. Furthermore, if sophisticated spread spectrum communications, e.g., fast frequency hopping, is considered, a synchronization circuit with fast and stable convergence performance has to be made for achieving the specified hopping performance.

Conventionally, the most well known synchronization loop design is analog phase lock loop (PLL) with added voltage controlled oscillator (VCO) and loop filter, or with direct digital synthesizer (DDS) [1-5]. But, nowadays, full digital PLL design methods and approaches with digital loop filters are also applied in many related fields for its inherent benefits [4]. The use of higher-order digital loop filter should generally be restricted to filtering purpose, as these designs can be slower than lower-order PLLs and may exhibit a lower phase margin. And if a fast-settling PLL application is desired, e.g., a fast frequency hopping circuit, it is appropriate to select a lower-order digital loop for its simplicity and flexibility [8-10]. The theoretic analysis and design of a PLL circuit is complicated, therefore, many design approaches based on some specific models or simulation tools are taken to evaluate system parameters in a fast manner [14-15] [6-7].

In this paper, a simple and direct scheme based on a pre-assured stable 2nd order digital loop filter for designing a carrier recovery circuit is developed, which can tell the designer the convergence area by simply adjusting or selecting two loop parameters in the whole design stages.

The remainder of this paper is organized as follows. In Section II, the basics for a pre-assured stable 2nd order digital loop design will be addressed thoroughly, which include its function block diagram, recursive formulations, transfer function, and convergence characteristics and responses with two simply adjusted parameters. In Section III and IV, two typical application cases with pre-assured stable 2nd order digital loop design, i.e., QPSK phase tracking and Radio frequency tracking, respectively, will be presented. Conclusion is in final Section V.

II. PRE-ASSURED 2ND ORDER DIGITAL LOOP FILTER

In this section, the function block diagram, recursive formulations, transfer function, and convergence triangle and response for a pure 2nd order digital loop filter design are addressed.

A. Function Block Diagram

Fig. 1 shows a typical synchronization function block diagram, which is consisted of the synchronization circuit and 2nd order digital loop filter with two adjustable C_1 and C_2 parameters. The synchronization circuit is labeled as $f(x)$=1 for analyzing the pure 2nd order digital loop filter only. The initial input signal δx_m value is $\delta x_0 = x_0$ and the feedback signals within this function diagram are updated periodically by system clocks. The C_1 and C_2 are the only two parameters which we can select to let δx_m converge to zero for a stable response. In this diagram, two internal small feedback loops are built for generating S_{m+1}, x_{m+1}, y_{m+1}, and many other

parameters for recursive formulations.

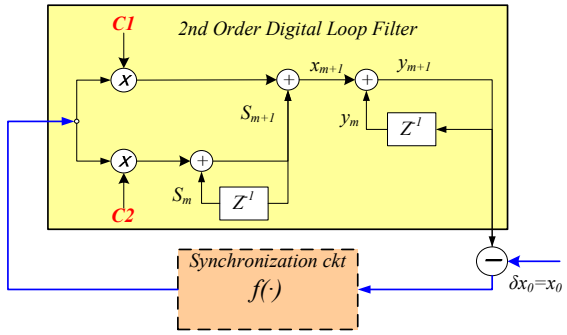

Fig. 1 The typical synchronization function block diagram with two adjustable C_1 and C_2 parameters from 2nd order digital loop filter

B. *Recursive Formulations*

The basic recursive formulations are derived from (1a) to (1d), respectively, based on the two internal feedback loops from **Fig. 1**.

$$S_{m+1} = C_2 \cdot \delta x_m + S_m , \quad (1a)$$

$$x_{m+1} = C_1 \cdot \delta x_m + S_{m+1} , \quad (1b)$$

$$y_{m+1} = y_m + x_{m+1} , \quad (1c)$$

$$\delta x_{m+1} = \delta x_0 - y_{m+1} \Rightarrow \delta x_m = \delta x_0 - y_m , \quad (1d)$$

where δx_m is the input difference quantity. Moreover, the transfer function $H(z)$ of this 2nd order digital loop filter with $f(x)$=1 is derived and shown in (2) by wrapping up and taking z-transform of (1a) to (1d).

$$H(z) = \frac{\delta x_m}{\delta x_0} = \frac{(z-1)^2}{z^2 + (C_1 + C_2 - 2)\cdot z + (1 - C_1)} \quad (2)$$

C. *Convergence Triangle*

The pure 2nd order digital loop filter will be stable if C_1 and C_2 parameters in the denominator of the $H(z)$ transfer function could satisfy the constrained stable conditions from Jury criteria [11-12], which is represented as

$$0 < C_1 < 2 \quad C_2 > 0 \quad 2C_1 + C_2 > 4 , \quad (3)$$

where these three different curves formed by C_1 and C_2 combinations will generate a convergence triangle. **Fig. 2** shows this theoretic syable convergence triangle based on (3).

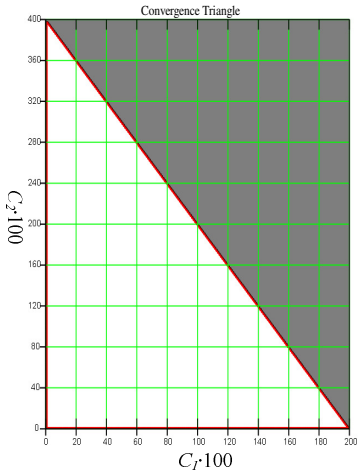

Fig. 2 Theoretic stable convergence triangle based on Jury criteria (C_1 is 0~2 and C_2 is 0~4)

Within this constrained region, the arbitrary combinations of C_1 and C_2 parameters will generate stable system responses only with the differences of clock cycles required to achieve stable conditions. **Fig. 3** shows the simulated convergence clock cycle contours with only 0.1% oscillating amplitude variations, i.e., the final amplitude variations to reach stable criteria is within 0.1%. If the combinations of C_1 and C_2 are in the inner contours, the clock time to reach stable criteria is shorter, i.e., it will reach stable condition more quickly. On the contrary, in the outer contours, the clock time to reach stable criteria is longer.

We can choose any combinations of C_1 and C_2 within this region to have a specific stable response. For example, within the inner constrained contour (grey color), the convergence clock cycles no more than ten (10) are required to reach the stable criteria of only 0.1% amplitude variations. In the same manner, for the outer pink contour the convergence clock cycles required will be increased to no more than twenty (20) whenever any combinations of C_1 and C_2 values within this contour are selected. Finally, near the edges of this convergence triangle, the convergent clock cycles will be much more than one hundred (100) cycles, which means the convergence speed to reach the stable criteria of 0.1% amplitude variations will be even slower and more sensitive.

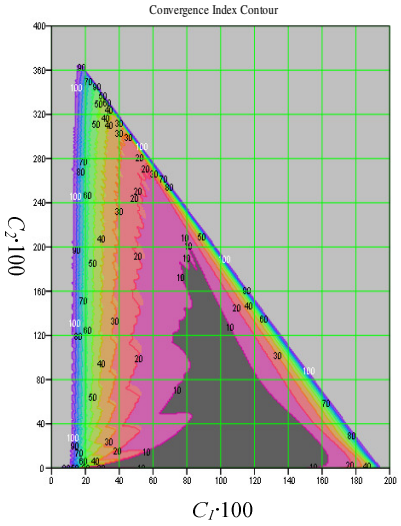

Fig. 3 Convergence clock cycle contour within 0.1% amplitude variations for stable criteria

D. *Convergence Response*

The δx_m convergence responses curves are shown in **Fig. 4**, where the x-axis represents the number of updating clock cycles (m) and the y-axis represents the δx_m amplitudes. The first combination takes about ten cycles to be stable, and the second one take at least 50 cycles to be settled down. But when C_1 and C_2 are selected near the edges of convergence triangle as shown in **Fig. 2** or **3**, e.g., C_1= C_2=0.19 combination, obviously it will need more clock cycles to converge or even become unstable if they are outside of this region. Therefore, the convergence speed simply depends on the choice of C_1 and C_2. If C_1 and C_2 are in the inner part of

the convergence triangle, it will converge more quickly; on the contrary, it will converge more slowly.

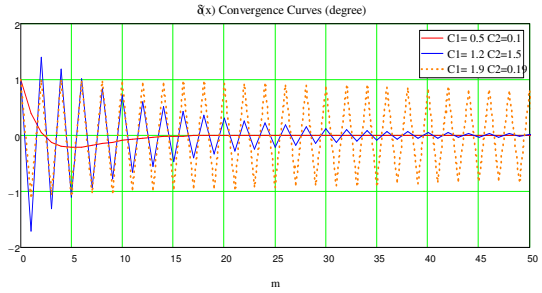

Fig. 4 Convergence response curves of 2nd order digital loop *with* three adjustable C_1 and C_2 combinations

III. QPSK PHASE TRACKING WITH PHASE ROTATOR

In this section, the function block diagram, recursive formulations, transfer function, and convergence response for a QPSK phase tracking circuit design are addressed.

A. *Function Block Diagram*

Fig. 5 shows the function block diagram of a QPSK phase tracking circuit consisted of phase rotator, phase discriminator, and the pre-assured 2nd order digital loop filter. This is a typical phase tracking system, where the initial phase shift (θ_0) and residue angular frequency (ω_r) from analog I and Q channel signals are mixed into this tracking system. The aim is, therefore, to correct the shifted signal phases by this tracking system. When this tracking loop works, the phase differences $\delta\theta$ will cause the phase rotator to rotate, and the two phase rotated signals J and P dependent on $\delta\theta$ values in each clock cycle will be input to the phase discriminator for a discriminated phase output. Thereafter, the two adjustable parameters C_1 and C_2 inside the pre-assured 2nd order digital loop filter are taken for a stable output performance according to the specified convergence triangle as aforementioned. The phase rotator can be implemented with SRAM chips or a FPGA chip in a table look-up style.

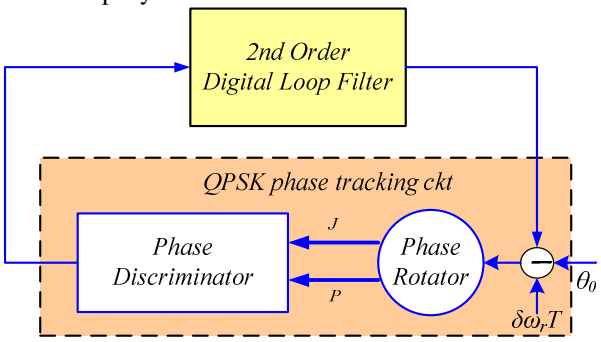

Fig. 5 Function block diagram of QPSK phase tracking circuit with phase rotator

B. *Recursive Formulations*

The basic recursive formulations based on **Fig. 1** and **Fig. 5** are derived from (3a) to (3d), respectively.

$$S_{m+1} = C_2 \cdot k_p f\left(\delta\theta_m\right) + S_m, \tag{3a}$$

$$x_{m+1} = C_1 \cdot k_p f\left(\delta\theta_m\right) + S_{m+1}, \tag{3b}$$

$$y_{m+1} = y_m + x_{m+1}, \tag{3c}$$

$$\delta\theta_m = \left(\theta_0 + \delta\omega_r mT\right) - y_m, \tag{3d}$$

where k_p is the approximated slope for linear phase discriminator output response; $\delta\theta_m$ is the m[th] phase tracking error; $f(\delta\theta_m)$ is phase discriminated output represented and approximated as (4) and (5), respectively [13].

$$f\left(\delta\theta_m\right) = J\left(\delta\theta_m\right)\mathrm{sgn}\left(P\left(\delta\theta_m\right)\right) - P\left(\delta\theta_m\right)\mathrm{sgn}\left(J\left(\delta\theta_m\right)\right) \tag{4}$$

$$f\left(\delta\theta_m\right) = \mathrm{mod}\left\langle\delta\theta_m, 2\pi\right\rangle - \frac{\pi}{2}\left\lfloor\frac{\delta\theta_m + \pi/4}{\pi/2}\right\rfloor \tag{5}$$

Fig. 6 shows the real phase discriminator characteristic curve (red solid) and approximated curve (blue dashed) with k_p slope, where $k_p = \frac{8}{\sqrt{2}\cdot\pi}$. This is basically a saw-tooth waveform with π/2 phase cycle. For no loss of generality, if |I |=|Q|=1 is assumed, it will be available for each possible case from (5) when QPSK constellations are considered.

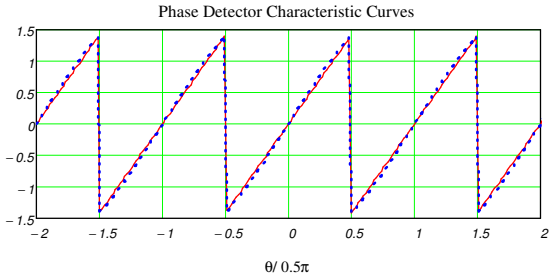

Fig. 6 Phase discriminator characteristic curves (red solid: real; blue dashed: approximated)

C. *Convergence Response*

Fig. 7 shows three different $\delta\theta_m$ convergence response curves by selecting three C_1 and C_2 combinations for QPSK phase tracking loop with residue frequency equal to -0.01 clock rate and initial phase of 135 degrees. The first combination takes about twenty cycles to be stable, and the second one take less than 10 cycles to be settled down. The third combination takes about at least 100 cycles to be within the specified 0.1% amplitude variations. The only convergence limitation is to keep the swing within a stable region, and it is always possible.

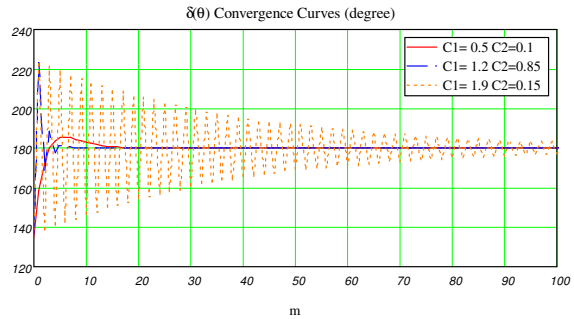

Fig. 7 Convergence response curves for *QPSK phase tracking loop* with three C_1 and C_2 combinations.

IV. RADIO FREQUENCY TRACKING WITH DDS

In this section, the function block diagram, recursive formulations, transfer function, and convergence response for a radio frequency tracking circuit design are addressed.

A. Function Block Diagram

Fig. 8 shows the function block diagram of a RF frequency tracking loop with DDS (direct digital synthesizer). This is a typical frequency tracking system, where the phase shift and residue angular frequency (ω_r) from analog I and Q channels are mixed into this tracking system. θ_0 is initial phase shift assumed and $\delta\omega T$ the phase tracking error in each clock cycle when this tracking loop works. The DDS output is the reference frequency of a synthesizer for even higher local frequency, i.e., if the reference frequency is f_r, the synthesizer frequency is $N f_r = f_l$. J and P are the two phase shifted signals dependent on $\delta\omega T$ values in each clock cycle. The input signal is radio frequency, its carrier is f_{rf}, the local angular frequency of demodulator is f_l, and $\delta\omega = 2\pi(f_{rf}-f_l)$, the aim of this circuit is to make $\delta\omega=0$ by changing f_l from DDS synthesizer output. The aim is then to correct the drifted signal frequencies by this tracking system consisted of DDS, A/D and demodulator, phase discriminator, and the pre-assured 2nd order digital loop filter.

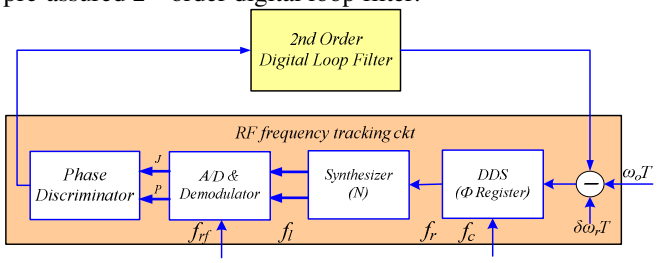

Fig. 8 Function block diagram of RF frequency tracking circuit with DDS

B. Recursive Formulations

The basic recursive formulations based on **Fig. 1** and **Fig. 8** are derived from (6a) to (6d), respectively.

$$S_{m+1} = C_2 \cdot Nk_d k_p f\left(\delta\omega_m T\right) + S_m, \quad (6a)$$

$$x_{m+1} = C_1 \cdot Nk_d k_p f\left(\delta\omega_m T\right) + S_{m+1}, \quad (6b)$$

$$\theta_{m+1} = \theta_m + \delta\omega_m T, \quad (6c)$$

$$\delta\omega_{m+1} = \delta\omega_0 - k_d \cdot x_{m+1}, \quad (6d)$$

where k_d is function of DDS clock frequency and phase register setting resolution, shown as $f_c/2^P$ (P is register resolution); k_p is the approximated slope for linear phase discriminator output response; $N f_r = f_l$.

C. Convergence Response

Fig. 9 shows three δf_m convergence response curves (in units of MHz) of Radio frequency tracking loop by setting residue frequency equal to 1% clock rate and initial phase equal to 135 degrees. The assumed update frequency $1/T$ is 10MHz. These three combinations take at most forty cycles to be settled down within the specified 0.1% amplitude variations.

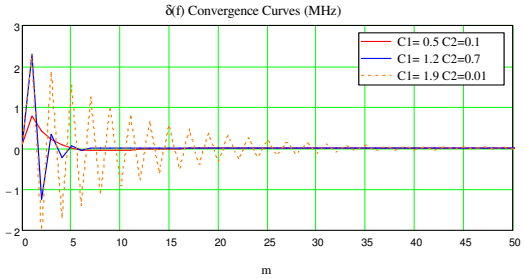

Fig. 9 Convergence response curve of RF frequency *tracking circuit with* three adjustable C_1 and C_2 combinations

V. CONCLUSION

In this paper, a pre-assured 2nd order digital loop filter with easily adjustable parameters for predicted stable convergence characteristics and responses is proposed. Moreover, the general recursive formulations and derived convergence triangle for the filter itself and its applications in phase and frequency variations are also presented. This simple and direct scheme can tell the designers the convergence regions by simply adjusting or selecting these parameter combinations in the whole design stages.

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